

**METHOD OF FORMING DUAL GATE INSULATOR
LAYERS FOR CMOS APPLICATIONS**

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to method used to fabricate semiconductor devices, and more specifically to a method used to form dual gate dielectric layers for specific applications of complimentary metal oxide semiconductor (CMOS), devices, wherein one of the gate dielectric layers is a silicon nitride layer.

(2) Description of Prior Art

Advanced CMOS designs are formed for multiple applications with each application requiring a specific CMOS type device, in turn necessitating the fabrication of different type CMOS devices on the same semiconductor chip. For example CMOS devices such as a device used for input/output (I/O) applications require thicker gate insulator layers for I/O operation than counterpart CMOS devices used for core memory applications, which in turn are used at lower operating voltages thus requiring thinner gate insulator layers. Therefore to satisfy the requirements of the different CMOS applications dual gate oxide processes have been used. The conventional method of forming dual gate oxide layers is to initially grow the thick insulator

TSMC02-066

component on an entire semiconductor substrate followed by removal of the thick insulator layer in the area of the semiconductor substrate requiring the thinner gate insulator layer. The thinner gate insulator layer is then regrown on the bare semiconductor region. However to insure quality of the regrown, thinner insulator layer, a pre-clean in a hydrofluoric acid containing solution should be used to remove native oxide from the region of the semiconductor substrate on which the thinner insulator layer will be regrown. If the pre-clean procedure is omitted the inclusion of the native oxide will degrade the quality of the regrown, thin insulator layer. However if the pre-clean procedure is employed the exposed thicker insulator layer will be thinned, perhaps to a point deleteriously influencing the performance or reliability of the I/O device featuring the thicker gate insulator component.

The present invention will describe a process for forming dual gate insulator layers in which a HF type pre-clean is applied prior to the formation of each gate insulator layer, made possible as a result of the insolubility of the exposed first gate insulator layer in the HF type solution. This allows for complete removal of native oxide from the surface of the semiconductor substrate prior to the growth of the second gate insulator layer, thus avoiding the inclusion of the lower dielectric quality native oxide in the second gate insulator layer. In addition this invention will describe a dual gate insulator process in which the thinner component is formed and exposed prior to formation of a thicker, second insulator layer. Prior art such as Okuno et al, in U.S. Pat. No. 6,110,842, Kepler, in U.S. Pat. No. 6,030,862, Tsui et al, in U.S. Pat. No. 5,960,289, Lutze et al, in U.S. Pat. No. 6,262,455 B1, and Buller et al, in U.S. Pat. No. 6,037,224, describe process sequences for attainment of dual gate insulator layers,

TSMC02-066

however none of the prior art describe the unique process sequence described in this present invention in which dual gate insulator layers are formed using an HF type solution prior to formation of each component of the dual gate insulator layer.

SUMMARY OF THE INVENTION

It is an object of this invention to provide a dual gate insulator layer process sequence to form a first gate insulator layer comprised with a first thickness, on a first region of a semiconductor substrate, followed by formation of a second gate insulator layer comprised with a second thickness, on a second region of the semiconductor substrate.

It is another object of this invention to apply a HF type pre-clean procedure prior to formation of each gate insulator layer, without degrading the thickness of the exposed first gate insulator layer during the application of a second HF type pre-clean procedure, applied prior to second gate insulator formation.

It is still another object of this invention to form a silicon nitride, first gate insulator layer in a first region of the semiconductor substrate, followed by the thermal growth of a thicker silicon dioxide, second gate insulator layer.

In accordance with the present invention a method of forming dual gate insulator layers on a semiconductor substrate, featuring the use of HF type pre-cleans applied prior to formation of each of the gate insulator layers, is described. After application of a first HF type pre-clean, a

TSMC02-066

thin silicon nitride layer is formed or deposited on the surface of a semiconductor substrate. Silicon nitride is selectively removed from the surface of a second region of the semiconductor substrate, with thin silicon nitride still remaining overlying the surface of a first region of the semiconductor substrate. After a second HF type pre-clean procedure a thermal oxidation procedure is performed resulting in the growth of a silicon dioxide gate insulator layer in the second region of the semiconductor substrate, with the thickness of the silicon dioxide gate insulator greater than the thickness of the unoxidized, silicon nitride layer located in the first region of the semiconductor substrate. The thermal oxidation procedure, performed at an elevated temperature, results in removal of bulk traps in the thin silicon nitride gate insulator layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiments with reference to the attached drawings that include:

Figs. 1 - 4, which schematically, in cross-sectional style, describe key fabrication stages employed to form dual gate insulator layers, each comprised of a specific thickness, featuring the use of HF type pre-cleans applied prior to formation of each of the gate insulator layers.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of forming dual gate insulator layers, each comprised of a specific thickness, featuring the use of HF type pre-cleans applied prior to formation of each of the gate insulator layers, will now be described in detail. Semiconductor substrate 3, comprised of P type, single crystalline silicon, featuring a <100> crystallographic orientation, is used and schematically shown in Fig. 1. Region 1, of semiconductor substrate 3, will be reserved for accommodation of I/O type, CMOS devices, wherein the I/O type devices will subsequently operate at higher voltages than counterpart core type CMOS devices, to subsequently be formed in region 2, of semiconductor substrate 3. Shallow trench isolation (STI), regions 4, comprised of silicon oxide filled shallow trench shapes, are formed for isolation between the I/O and core devices, as well as to isolate and define specific active device regions of each type CMOS device. This is schematically shown in Fig. 1.

Prior to formation of a first gate insulator layer a first pre-clean procedure, performed using a solution containing an HF component, is employed. The solution used for the first pre-clean procedure can be a buffered HF solution, buffered by the inclusion of an ammonium fluoride component, or the solution can be a dilute HF solution, diluted via the use of addition of a de-ionized water component. If desired the first pre-clean procedure can be accomplished via a vapor HF procedure, performed in situ in the same chamber of tool to be subsequently used for a silicon nitride deposition. After the first pre-clean procedure removing native oxide from the entire surface of semiconductor substrate 3, silicon nitride layer 5a, is formed. Silicon nitride

TSMC02-066

layer 5a, formed on the native oxide free semiconductor surface, is obtained at a thickness between about 5 to 30 Angstroms via use of either direct plasma nitridization procedures, direct thermal nitridation procedures, or chemical vapor deposition (CVD), procedures. Silicon nitride layer 5a, which will be used as the thin gate dielectric layer of core type CMOS devices, can also be obtained at a thickness between about 5 to 30 Angstroms, via rapid thermal chemical vapor deposition (RTCVD), via remote plasma enhanced chemical vapor deposition (RPCVD), or via atomic layer chemical vapor deposition (ALCVD), procedures. The result of the silicon nitride formation is schematically shown in Fig. 2.

Silicon nitride layer 5a, will remain on semiconductor substrate 3, in core region 2, while I/O region 1, will be prepared for formation of a thicker gate insulator layer. Photoresist shape 6, is defined and used as an etch mask to protect silicon nitride layer 5a, from a procedure used to remove the portion of silicon nitride layer 5a, from the surface of semiconductor substrate 3, in I/O region 1. This can be accomplished selectively via use of a hot phosphoric acid solution which etches silicon nitride while the phosphoric acid procedure selectively terminates at the appearance of the top surface of semiconductor substrate 3. If desired selective removal of silicon nitride can be accomplished via dry etching procedures, using CF_4 or Cl_2 as a selective etchant for silicon nitride. The result of this procedure, featuring thin silicon nitride gate insulator layer 5a, only in core region 2, is schematically shown in Fig. 3.

Removal of photoresist shape 6, is accomplished via plasma oxygen ashing procedures, with this procedure forming an unwanted native oxide layer, (not shown in the drawings), on the

TSMC02-066

exposed surface of semiconductor substrate 3, in I/O region 1. If the native oxide is not removed it will be incorporated into a subsequently regrown second gate insulator layer, with the inclusion of the native oxide resulting in decreased dielectric integrity of the regrown second gate insulator layer. Therefore a second pre-clean procedure is performed prior to growth of a second gate insulator layer, with the second pre-clean procedure again using an HF component to remove native oxide. Again as was the case with the first pre-clean procedure a wet etch solution such as a buffered HF solution, buffered by the inclusion of an ammonia fluoride component, or an HF solution, diluted via the use of addition of a de-ionized water component, can be used. If desired the second pre-clean procedure can be again be accomplished via a vapor HF procedure, performed in situ in the same chamber to be used for growth of a second gate insulator layer. Of utmost importance is the presence of silicon nitride as the first gate insulator layer. Silicon nitride gate insulator layer 5a, is not etched via exposure to the HF type environments during the second pre-clean procedure. If the first gate insulator layer in core region 2, were comprised of silicon dioxide, native oxide located on I/O region 1, could not have been removed via HF type procedures.

Formation of second gate insulator layer 7, comprised of silicon dioxide, is next accomplished and schematically shown in Fig. 4. Silicon dioxide layer 7, is obtained at a thickness between about 30 to 80 Angstroms via thermal oxidation procedures. If desired second gate insulator layer 7, can be obtained at the same thickness, between about 30 to 80 Angstroms, via plasma oxidation procedures. The formation of second gate insulator layer 7, in I/O region 1, at a thickness greater than the thickness of first gate insulator 5a, via thermal or plasma

procedures, also results in removal of bulk traps in silicon nitride, resulting in a trap free, silicon nitride, first gate insulator layer 5b, shown schematically in Fig. 4. Therefore the thermal budget using the formation of second gate insulator layer 7, in combination with annealing of first gate insulator layer 5b, is reduced when compared to counterpart process sequences in which these procedures, formation of a second gate insulator and annealing of a first gate insulator layer, are performed separately.

If desired the present invention can be used to form multiple insulator layers, each with a specific thickness, for three or more gate insulator applications, with a HF type pre-clean performed prior to each gate insulator formation. This is accomplished via formation of a first silicon nitride gate insulator layer in a first region of a semiconductor substrate, comprised with a partial thickness of silicon nitride. After an HF pre-clean procedure deposition of a second silicon nitride layer on the pre-cleaned portion of semiconductor substrate results in a final thickness for the first silicon nitride thickness while the additional silicon nitride deposition results in a second silicon nitride gate insulator layer in the second semiconductor substrate region. After removal of the second silicon nitride layer from the surface of a third region of the semiconductor substrate, another HF type pre-clean procedure is applied followed by the growth of a third gate insulator layer, a silicon dioxide layer, on the third region of the semiconductor substrate.

TSMC02-066

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is: